

LMK01000/LMK01010/LMK01020

1.6 GHz High Performance Clock Buffer, Divider, and Distributor

General Description

The LMK01000/LMK01010/LMK01020 family provides an easy way to divide and distribute high performance clock signals throughout the system. These devices provide best-in-class noise performance and are designed to be pin-to-pin and footprint compatible with LMK03000/LMK02000 family of precision clock conditioners.

The LMK01000/LMK01010/LMK01020 family features two programmable clock inputs (CLKin0 and CLKin1) that allow the user to dynamically switch between different clock domains.

Each device features 8 clock outputs with independently programmable dividers and delay adjustments. The outputs of the device can be easily synchronized by an external pin (SYNC*).

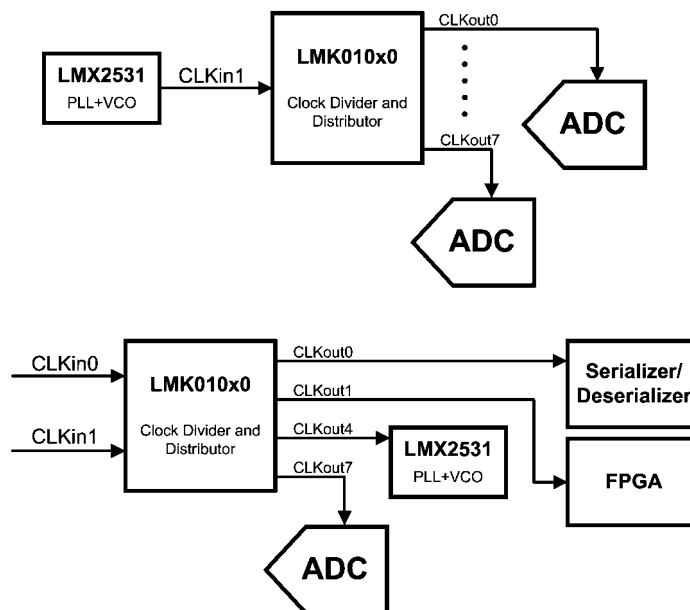
Target Applications

- High performance Clock Distribution
- Wireless Infrastructure
- Medical Imaging
- Wired Communications
- Test and Measurement
- Military / Aerospace

Features

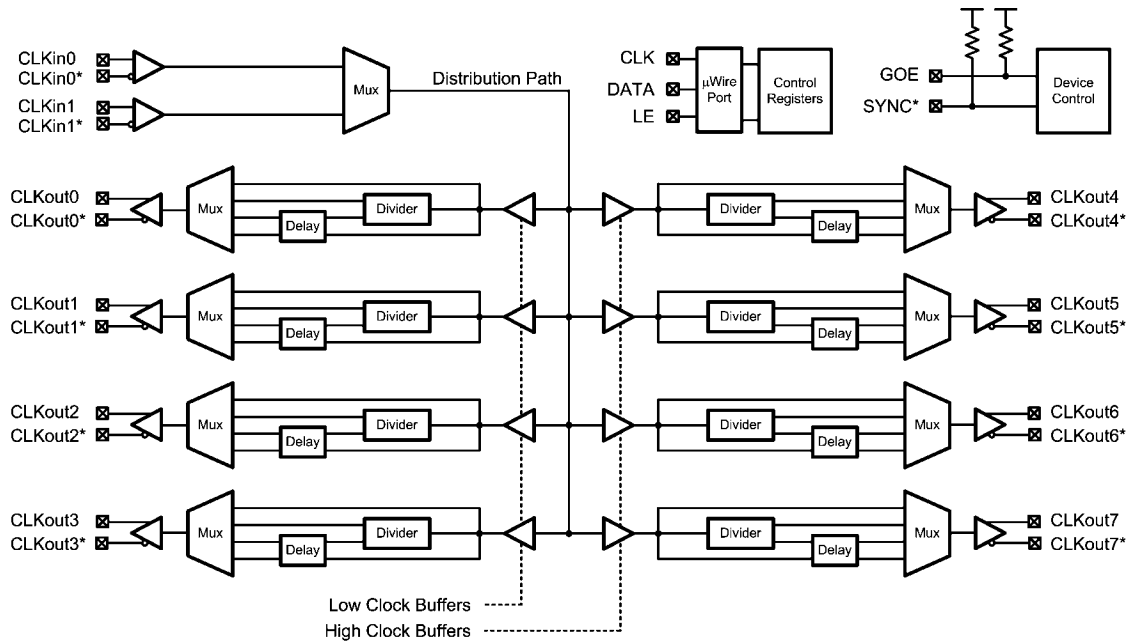
- 30 fs additive jitter (100 Hz to 20 MHz)
- Dual clock inputs
- Programmable output channels (0 to 1600 MHz)
 - LMK01000: 3 LVDS outputs (CLKout0 - CLKout2) + 5 LVPECL outputs (CLKout3 - CLKout7)
 - LMK01010: 8 LVDS outputs
 - LMK01020: 8 LVPECL outputs
 - Channel divider values of 1, 2 to 510 (even divides)
 - Programmable output skew control
- External synchronization
- Pin compatible family of clocking devices
- 3.15 to 3.45 V operation
- Package: 48 pin LLP (7.0 x 7.0 x 0.8 mm)

System Diagram



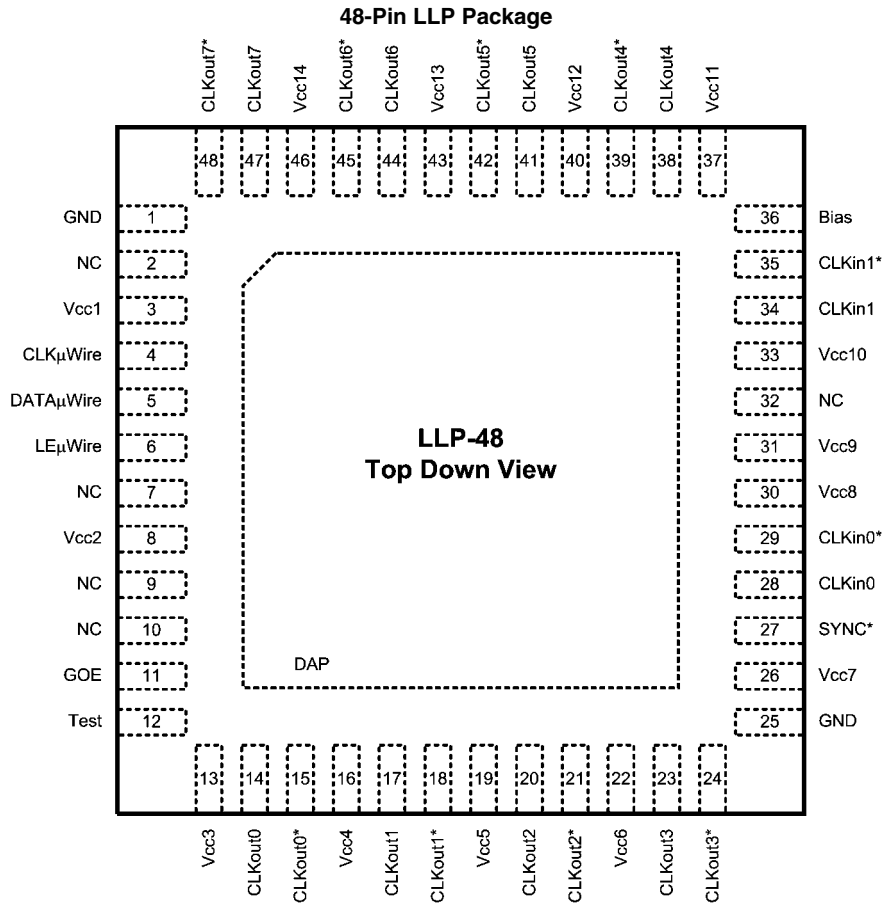
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Functional Block Diagram



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Connection Diagram



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Pin Descriptions

Pin #	Pin Name	I/O	Description
1, 25	GND	-	Ground
2, 7, 9, 10, 32	NC	-	No Connect. Pin is not connected to the die.
3, 8, 13, 16, 19, 22, 26, 30, 31, 33, 37, 40, 43, 46	Vcc1, Vcc2, Vcc3, Vcc4, Vcc5, Vcc6, Vcc7, Vcc8, Vcc9, Vcc10, Vcc11, Vcc12, Vcc13, Vcc14	-	Power Supply
4	CLKuWire	I	MICROWIRE Clock Input
5	DATAuWire	I	MICROWIRE Data Input
6	LEuWire	I	MICROWIRE Latch Enable Input
11	GOE	I	Global Output Enable
12	Test	O	This is an output pin used strictly for test purposes and should be not connected for normal operation. However, any load of an impedance of more than 1 k Ω is acceptable.
14, 15	CLKout0, CLKout0*	O	Clock Output 0
17, 18	CLKout1, CLKout1*	O	Clock Output 1
20, 21	CLKout2, CLKout2*	O	Clock Output 2
23, 24	CLKout3, CLKout3*	O	Clock Output 3
27	SYNC*	I	Global Clock Output Synchronization
28, 29	CLKin0, CLKin0*	I	CLKin 0 Input; Must be AC coupled
34, 35	CLKin1, CLKin1*	I	CLKin 1 Input; Must be AC coupled
36	Bias	I	Bias Bypass
38, 39	CLKout4, CLKout4*	O	Clock Output 4
41, 42	CLKout5, CLKout5*	O	Clock Output 5
44, 45	CLKout6, CLKout6*	O	Clock Output 6
47, 48	CLKout7, CLKout7*	O	Clock Output 7
DAP	DAP	-	Die Attach Pad should be connected to ground.

The LMK01000 family is footprint compatible with the LMK03000/02000 family of devices. All CLKout pins are pin-to-pin compatible, and CLKin0 and CLKin1 are equivalent to OSCin and Fin, respectively .

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Parameter	Symbol	Ratings	Units
Power Supply Voltage	V_{CC}	-0.3 to 3.6	V
Input Voltage	V_{IN}	-0.3 to ($V_{CC} + 0.3$)	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Lead Temperature (solder 4 s)	T_L	+260	°C
Junction Temperature	T_J	125	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Ambient Temperature	T_A	-40	25	85	°C
Power Supply Voltage	V_{CC}	3.15	3.3	3.45	V

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: This device is a high performance integrated circuit with ESD handling precautions. Handling of this device should only be done at ESD protected work stations. The device is rated to a HBM-ESD of > 2 kV, a MM-ESD of > 200 V, and a CDM-ESD of > 1.2 kV.

Package Thermal Resistance

Package	θ_{JA}	θ_{J-PAD} (Thermal Pad)
48-Lead LLP (Note 3)	27.4° C/W	5.8° C/W

Note 3: Specification assumes 16 thermal vias connect the die attach pad to the embedded copper plane on the 4-layer JEDEC board. These vias play a key role in improving the thermal performance of the LLP. It is recommended that the maximum number of vias be used in the board layout.

Electrical Characteristics (Note 4)

(3.15 V \leq V_{CC} \leq 3.45 V, -40 °C \leq T_A \leq 85 °C, Differential Inputs/Outputs; except as specified. Typical values represent most likely parametric norms at V_{CC} = 3.3 V, T_A = 25 °C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Current Consumption						
I_{CC}	Power Supply Current (Note 5)	All outputs enabled, no divide or delay (CLKoutX_MUX = Bypassed)	LMK01000		271	mA
			LMK01010		160	
		Per channel, no divide or delay (CLKoutX_MUX = Bypassed)	LMK01020		338	
			LVDS		17.8	
		LVPECL (Includes Emitter Resistors)		40		
I_{CCPD}	Power Down Current	POWERDOWN = 1		1		
CLKin0, CLKin0*, CLKin1, CLKin1*						
f_{CLKin}	CLKin Frequency Range		1		1600	MHz
$SLEW_{CLKin}$	CLKin Frequency Input Slew Rate	(Notes 6, 8)	0.5			V/ns
$DUTY_{CLKin}$	CLKin Frequency Input Duty Cycle	$f_{CLKin} \leq 800$ MHz	30		70	%
		$f_{CLKin} > 800$ MHz	40		60	
P_{CLKin}	Input Power Range for CLKin or CLKin*	AC coupled	-13		5	dBm

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
Clock Distribution Section--Delays							
Delay _{CLKout}	Maximum Allowable Delay(Note 8)	f _{CLKoutX} ≤ 1 GHz (Delay is limited to maximum programmable value)			2250	ps	
		f _{CLKoutX} > 1 GHz (Delay is limited to 1/2 of a period)			0.5/ f _{CLKoutX}		
Clock Distribution Section - Divides							
Divide _{CLKoutX}	Allowable divide range. (Note that 1 is the only allowable odd divide value)	f _{CLKinX} ≤ 1300 MHz	1		510	n/a	
		1300 MHz < f _{CLKinX} ≤ 1600 MHz	1		2		
Clock Distribution Section - LVDS Clock Outputs							
Jitter _{ADD}	Additive RMS Jitter (Note 7)	R _L = 100 Ω Bandwidth = 100 Hz to 20 MHz Vboost = 1	f _{CLKoutX} = 200 MHz		80	fs	
			f _{CLKoutX} = 800 MHz		30		
			f _{CLKoutX} = 1600 MHz		25		
Noise Floor	Divider Noise Floor(Note 7)	R _L = 100 Vboost = 1	f _{CLKoutX} = 200 MHz		-156	dBc/Hz	
			f _{CLKoutX} = 800 MHz		-153		
			f _{CLKoutX} = 1600 MHz		-148		
t _{SKEW}	CLKoutX to CLKoutY (Note 8)	Equal loading and identical clock configuration R _L = 100 Ω	-30	±4	30	ps	
V _{OD}	Differential Output Voltage	(Note 9)	Vboost=0	250	350	450	mV
			Vboost=1		390		
ΔV _{OD}	Change in magnitude of V _{OD} for complementary output states	R _L = 100 Ω	-50		50	mV	
V _{OS}	Output Offset Voltage	R _L = 100 Ω	1.070	1.25	1.370	V	
ΔV _{OS}	Change in magnitude of V _{OS} for complementary output states	R _L = 100 Ω	-35		35	mV	
I _{SA} I _{SB}	Clock Output Short Circuit Current single ended	Single ended outputs shorted to GND	-24		24	mA	
I _{SAB}	Clock Output Short Circuit Current differential	Complementary outputs tied together	-12		12	mA	

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
Clock Distribution Section - LVPECL Clock Outputs							
Jitter _{ADD}	Additive RMS Jitter(Note 7)	R _L = 100 Ω Bandwidth = 100 Hz to 20 MHz Vboost = 1	f _{CLKoutX} = 200 MHz		65	fs	
			f _{CLKoutX} = 800 MHz		25		
			f _{CLKoutX} = 1600 MHz		25		
Noise Floor	Divider Noise Floor(Note 7)	R _L = 100 Vboost = 1	f _{CLKoutX} = 200 MHz		-158	dBc/Hz	
			f _{CLKoutX} = 800 MHz		-154		
			f _{CLKoutX} = 1600 MHz		-148		
t _{SKEW}	CLKoutX to CLKoutY (Note 8)	Equal loading and identical clock configuration Termination = 50 Ω to Vcc - 2 V	-30	±3	30	ps	
V _{OH}	Output High Voltage	Termination = 50 Ω to Vcc - 2 V		Vcc - 0.98		V	
V _{OL}	Output Low Voltage			Vcc - 1.8		V	
V _{OD}	Differential Output Voltage	(Note 9)	Vboost = 0	660	810	965	mV
			Vboost = 1		865		
Digital LVTTTL Interfaces (Note 10)							
V _{IH}	High-Level Input Voltage		2.0		Vcc	V	
V _{IL}	Low-Level Input Voltage				0.8	V	
I _{IH}	High-Level Input Current	V _{IH} = Vcc	-5.0		5.0	μA	
I _{IL}	Low-Level Input Current	V _{IL} = 0	-40.0		5.0	μA	
V _{OH}	High-Level Output Voltage	I _{OH} = +500 μA	Vcc - 0.4			V	
V _{OL}	Low-Level Output Voltage	I _{OL} = -500 μA			0.4	V	

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital MICROWIRE Interfaces (Note 11)						
V_{IH}	High-Level Input Voltage		1.6		V_{CC}	V
V_{IL}	Low-Level Input Voltage				0.4	V
I_{IH}	High-Level Input Current	$V_{IH} = V_{CC}$	-5.0		5.0	μA
I_{IL}	Low-Level Input Current	$V_{IL} = 0$	-5.0		5.0	μA
MICROWIRE Timing						
t_{CS}	Data to Clock Set Up Time	See Data Input Timing	25			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	8			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	25			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	25			ns
t_{ES}	Clock to Enable Set Up Time	See Data Input Timing	25			ns
t_{CES}	Enable to Clock Set Up Time	See Data Input Timing	25			ns
t_{EWH}	Enable Pulse Width High	See Data Input Timing	25			ns

Note 4: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 5: See section 3.2 for more current consumption / power dissipation calculation information.

Note 6: For all frequencies the slew rate, $SLEW_{CLKin1}$, is measured between 20% and 80%.

Note 7: The noise floor of the divider is measured as the far out phase noise of the divider. Typically this offset is 40 MHz, but for lower frequencies this measurement offset can be as low as 5 MHz due to measurement equipment limitations. If the delay is used, then use section 1.3.

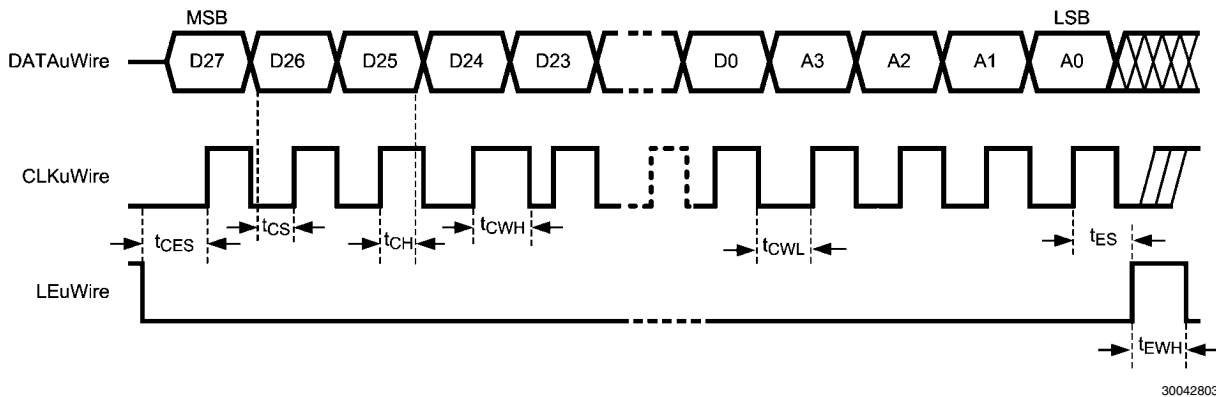
Note 8: Specification is guaranteed by characterization and is not tested in production.

Note 9: See characterization plots to see how this parameter varies over frequency.

Note 10: Applies to GOE, LD, and SYNC*.

Note 11: Applies to CLKuWire, DATAuWire, and LEuWire.

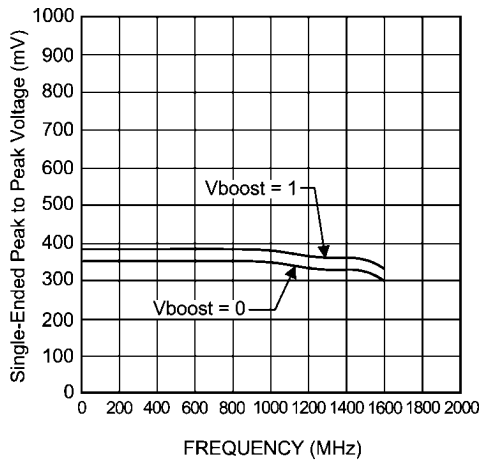
Serial Data Timing Diagram



Data bits set on the DATAuWire signal are clocked into a shift register, MSB first, on each rising edge of the CLKuWire signal. On the rising edge of the LEuWire signal, the data is sent from the shift register to the addressed register determined by the LSB bits. After the programming is complete the CLKuWire, DATAuWire, and LEuWire signals should be returned to a low state. The slew rate of CLKuWire, DatauWire, and LEuWire should be at least 30 V/ μs .

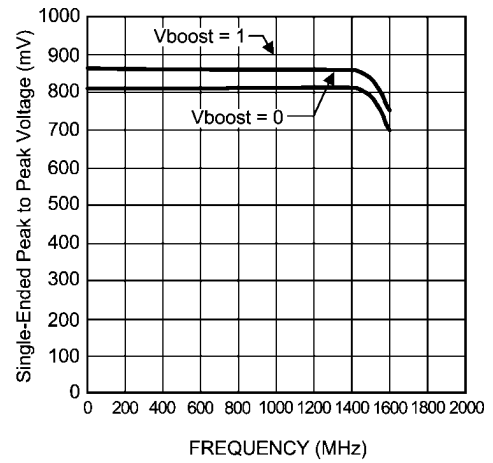
Typical Performance Characteristics

LVDS Single-Ended Peak to Peak Voltage



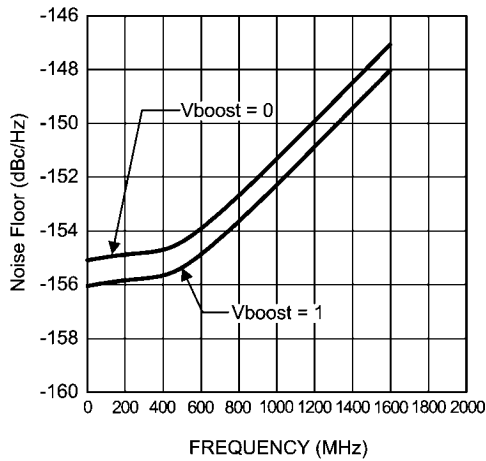
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LVPECL Single-Ended Peak to Peak Voltage



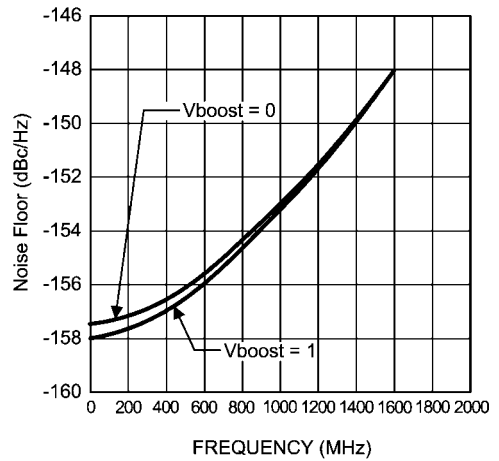
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LVDS Output Noise Floor



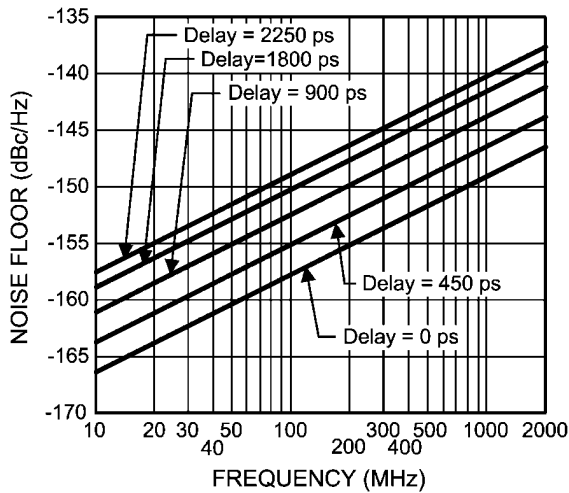
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LVPECL Output Noise Floor



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Delay Noise Floor (Adds to Output Noise Floor)



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1.0 Functional Description

The LMK010X0 family of clock distribution devices include a programmable divider, a phase synchronization circuit, a programmable delay, a clock output mux, and an LVDS or LVPECL output buffer in each channel. This allows multiple integer-related and phase-adjusted copies of the reference to be distributed to up to eight system components.

This family of devices comes in a 48-pin LLP package that is pin-to-pin and footprint compatible with other LMK02000/LMK03000 family of clocking devices.

1.1 BIAS PIN

To properly use the device, bypass Bias (pin 36) with a low leakage 1 μ F capacitor connected to Vcc. This is important for low noise performance.

1.2 CLKin0/CLKin0* and CLKin1/CLKin1 INPUT PORTS

The device can be driven either by the CLKin0/CLKin0* or the CLKin1/CLKin1* pins. The choice of which one to use is software selectable. These input ports must be AC coupled. To drive these inputs in a single ended fashion, AC ground the complementary input with a 0.1 μ F capacitor.

1.3 CLKout DELAYS

Each individual clock output includes a delay adjustment. Clock output delay registers (CLKoutX_DLY) support a 150 ps step size and range from 0 to 2250 ps of total delay. When the delay is enabled it adds to the output noise floor; the total additive noise is $10(\log(10^{(Output\ Noise\ Floor/10)} + 10^{(Delay\ Noise\ Floor/10)}))$. Refer to the Typical Performance Characteristics plots for the Delay Noise Floor information.

1.4 LVDS/LVPECL OUTPUTS

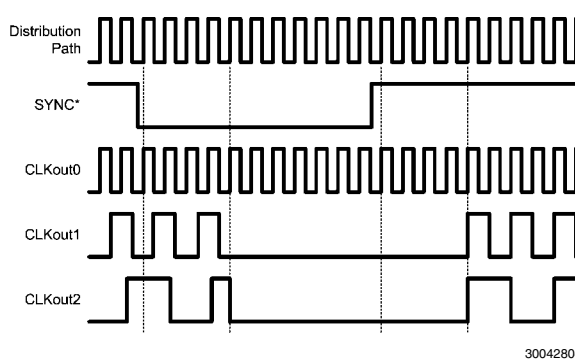
Each LVDS or LVPECL output may be disabled individually by programming the CLKoutX_EN bits. All the outputs may be disabled simultaneously by pulling the GOE pin low or programming EN_CLKout_Global to 0.

1.5 GLOBAL CLOCK OUTPUT SYNCHRONIZATION

The SYNC* pin synchronizes the clock outputs. When the SYNC* pin is held in a logic low state, the divided outputs are also held in a logic low state. When the SYNC* pin goes high, the divided clock outputs are activated and will transition to a high state simultaneously. Clocks in the Bypassed state are not affected by SYNC* and are always synchronized with the divided outputs.

The SYNC* pin must be held low for greater than one clock cycle of the Frequency Input port, also known as the distribution path. Once this low event has been registered, the outputs will not reflect the low state for four more cycles. When the SYNC* pin becomes high, the outputs will not simultaneously transition high until four more distribution path clock cycles have passed. See the SYNC* timing diagram for further detail. In the timing diagram below the clocks are programmed as CLKout0_MUX = Bypassed, CLKout1_MUX = Divided, CLKout1_DIV = 2, CLKout2_MUX = Divided, and CLKout2_DIV = 4.

SYNC* Timing Diagram



The SYNC* pin provides an internal pull-up resistor as shown on the functional block diagram. If the SYNC* pin is not terminated externally the clock outputs will operate normally. If the SYNC* function is not used, clock output synchronization is not guaranteed.

1.6 CONNECTION TO LVDS OUTPUTS

LMK01000/10 LVDS outputs can be connected in AC or DC coupling configurations; however, in DC coupling configuration, proper conditions must be presented by the LVDS receiver. To ensure such conditions, we recommend the usage of LVDS receivers without fail-safe or internal input bias such as DS90LV110T. LMK01000/10 LVDS drivers will provide the adequate DC bias for the LVDS receiver. We recommend AC coupling when using LVDS receivers with fail-safe or internal input bias.

1.7 CLKout OUTPUT STATES

Each clock output may be individually enabled with the CLKoutX_EN bits. Each individual output enable control bit is gated with the Global Output Enable input pin (GOE) and the Global Output Enable bit (EN_CLKout_Global).

All clock outputs can be disabled simultaneously if the GOE pin is pulled low by an external signal or EN_CLKout_Global is set to 0.

CLKoutX_EN bit	EN_CLKout_Global bit	GOE pin	Clock X Output State
1	1	Low	Low
Don't care	0	Don't care	Off
0	Don't care	Don't care	Off
1	1	High / No Connect	Enabled

When an LVDS output is in the Off state, the outputs are at a voltage of approximately 1.5 volts. When an LVPECL output is in the Off state, the outputs are at a voltage of approximately 1 volt.

1.8 GLOBAL OUTPUT ENABLE

The GOE pin provides an internal pull-up resistor. If it is not terminated externally, the clock output states are determined by the Clock Output Enable bits (CLKoutX_EN) and the EN_CLKout_Global bit.

1.9 POWER-ON-RESET

When supply voltage to the device increases monotonically from ground to Vcc, the power-on-reset circuit sets all registers to their default values, which are specified in the General Programming Information section. Voltage should be applied to all Vcc pins simultaneously.

2.0 General Programming Information

The LMK01000/LMK01010/LMK01020 device is programmed using several 32-bit registers which control the device's operation. The registers consist of a data field and an address field. The last 4 register bits, ADDR[3:0] form the address field. The remaining 28 bits form the data field DATA [27:0].

During programming, LEuWire is low and serial data is clocked in on the rising edge of clock (MSB first). When LEuWire goes high, data is transferred to the register bank selected by the address field. Only registers R0 to R7 and R14 need to be programmed for proper device operation.

It is required to program register R14.

2.1 RECOMMENDED PROGRAMMING SEQUENCE

The recommended programming sequence involves programming R0 with the reset bit set (RESET = 1) to ensure the device is in a default state. It is not necessary to program R0 again, but if R0 is programmed again, the reset bit is programmed clear (RESET = 0). An example programming sequence is shown below.

- Program R0 with the reset bit set (RESET = 1). This ensures the device is in a default state. When the reset bit is set in R0, the other R0 bits are ignored.
 - If R0 is programmed again, the reset bit is programmed clear (RESET = 0).
- Program R0 to R7 as necessary with desired clocks with appropriate enable, mux, divider, and delay settings.
- Program R14 with global clock output bit, power down setting.
 - R14 must be programmed in accordance with the register map as shown in the register map (see 2.2).

2.2 LMK01000/LMK01010/LMK01020 REGISTER MAP

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
	Data [27:0]																A3	A2	A1	A0															
R0	RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout0_EN	CLKout0_MUX [1:0]	CLKout0_DIV [7:0]	CLKout0_DLY [3:0]	0	0	0	0	0	0	0	0	0	0	0	0			
R1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout1_EN	CLKout1_MUX [1:0]	CLKout1_DIV [7:0]	CLKout1_DLY [3:0]	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout2_EN	CLKout2_MUX [1:0]	CLKout2_DIV [7:0]	CLKout2_DLY [3:0]	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout3_EN	CLKout3_MUX [1:0]	CLKout3_DIV [7:0]	CLKout3_DLY [3:0]	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout4_EN	CLKout4_MUX [1:0]	CLKout4_DIV [7:0]	CLKout4_DLY [3:0]	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout5_EN	CLKout5_MUX [1:0]	CLKout5_DIV [7:0]	CLKout5_DLY [3:0]	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout6_EN	CLKout6_MUX [1:0]	CLKout6_DIV [7:0]	CLKout6_DLY [3:0]	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKout7_EN	CLKout7_MUX [1:0]	CLKout7_DIV [7:0]	CLKout7_DLY [3:0]	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
R9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	Vbo_ost	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
R14	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKin_SELECT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
																EN_CLKout_Global	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
																POWERDOWN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

2.3 REGISTER R0 to R7

Registers R0 through R7 control the eight clock outputs. Register R0 controls CLKout0, Register R1 controls CLKout1, and so on. There is one additional bit in register R0 called RESET.

Aside from this, the functions of these bits are identical. The X in CLKoutX_MUX, CLKoutX_DIV, CLKoutX_DLY, and CLKoutX_EN denote the actual clock output which may be from 0 to 7.

Default Register Settings after Power-on-Reset

Bit Name	Default Bit Value	Bit State	Bit Description	Register	Bit Location
RESET	0	No reset, normal operation	Reset to power on defaults	R0	31
CLKoutX_MUX	0	Bypassed	CLKoutX mux mode	R0 to R7	18:17
CLKoutX_EN	0	Disabled	CLKoutX enable		16
CLKoutX_DIV	1	Divide by 2	CLKoutX clock divide		15:8
CLKoutX_DLY	0	0 ps	CLKoutX clock delay		7:4
CLKin_SELECT	0	CLKin1	Select CLKin0 or CLKin1		28
EN_CLKout_Global	1	Normal - CLKouts normal	Global clock output enable	R14	27
POWERDOWN	0	Normal - Device active	Device power down		26

2.3.1 RESET Bit -- R0 only

This bit is only in register R0. The use of this bit is optional and it should be set to '0' if not used. Setting this bit to a '1' forces all registers to their power-on-reset condition and therefore automatically clears this bit. If this bit is set, all other R0 bits are ignored and R0 needs to be programmed again if used with its proper values and RESET = 0.

2.3.2 CLKoutX_MUX[1:0] -- Clock Output Multiplexers

These bits control the Clock Output Multiplexer for each clock output. Changing between the different modes changes the blocks in the signal path and therefore incurs a delay relative to the Bypassed mode. The different MUX modes and associated delays are listed below.

CLKoutX_MUX [1:0]	Mode	Added Delay Relative to Bypassed Mode
0	Bypassed (default)	0 ps
1	Divided	100 ps
2	Delayed	400 ps (In addition to the programmed delay)
3	Divided and Delayed	500 ps (In addition to the programmed delay)

2.3.3 CLKoutX_DIV[7:0] -- Clock Output Dividers

These bits control the clock output divider value. In order for these dividers to be active, the respective CLKoutX_MUX (See 2.3.2) bit must be set to either "Divided" or "Divided and Delayed" mode. After all the dividers are programmed, the SYNC* pin must be used to ensure that all edges of the clock outputs are aligned (See 1.7). By adding the divider block to the output path a fixed delay of approximately 100 ps is incurred.

The actual Clock Output Divide value is twice the binary value programmed as listed in the table below.

CLKoutX_DIV[7:0]								Clock Output Divider value
0	0	0	0	0	0	0	0	Invalid
0	0	0	0	0	0	0	1	2 (default)
0	0	0	0	0	0	1	0	4
0	0	0	0	0	0	1	1	6
0	0	0	0	0	1	0	0	8
0	0	0	0	0	1	0	1	10
.
1	1	1	1	1	1	1	1	510

2.3.4 CLKoutX_DLY[3:0] -- Clock Output Delays

These bits control the delay stages for each clock output. In order for these delays to be active, the respective CLKoutX_MUX (See 2.3.2) bit must be set to either "Delayed" or "Divided and Delayed" mode. By adding the delay block to the output path a fixed delay of approximately 400 ps is incurred in addition to the delay shown in the table below.

CLKoutX_DLY[3:0]	Delay (ps)
0	0 (default)
1	150
2	300
3	450
4	600
5	750
6	900
7	1050
8	1200
9	1350
10	1500
11	1650
12	1800
13	1950
14	2100
15	2250

2.3.5 CLKoutX_EN bit -- Clock Output Enables

These bits control whether an individual clock output is enabled or not. If the EN_CLKout_Global bit is set to zero or if GOE pin is held low, all CLKoutX_EN bit states will be ignored and all clock outputs will be disabled.

CLKoutX_EN bit	Conditions	CLKoutX State
0	EN_CLKout_Global bit = 1	Disabled (default)
1	GOE pin = High / No Connect 1	Enabled

2.4 REGISTER R9 and R14

The LMK01000 family requires register R14 to be programmed as shown in the register map (see 2.2). R9 only needs to be programmed if Vboost is set to 1.

2.4.1 Vboost - Voltage Boost Bit

Enabling this bit sets all clock outputs in voltage boost mode which increases the voltage at these outputs. This can improve the noise floor performance of the output, but also increases current consumption, and can cause the outputs to be too high to meet the LVPECL/LVDS specifications.

Vboost bit	$f_{\text{CLKoutX}} < 1300$ MHz	$1300 \text{ MHz} \leq f_{\text{CLKoutX}} < 1500 \text{ MHz}$	$1500 \text{ MHz} \leq f_{\text{CLKoutX}} \leq 1600 \text{ MHz}$
0	Recommended to hit voltage level specifications for LVPECL/LVDS	Insufficient voltage level for LVDS/LVPECL specifications, but saves current	
1	Voltage May overdrive LVPECL/LVDS specifications, but noise floor is about 2-4 dB better and current consumption is increased	Voltage is sufficient for LVDS/LEVPECL specifications. Current consumption is increased, but noise floor is about the same.	Insufficient voltage for LVDS/LVPECL specifications, but still higher than when Vboost=0. Increased current consumption.

2.4.2 POWERDOWN Bit -- Device Power Down

This bit can power down the device. Enabling this bit powers down the entire device and all blocks, regardless of the state of any of the other bits or pins.

POWERDOWN bit	Mode
0	Normal Operation (default)
1	Entire Device Powered Down

2.4.3 INPUT_MUX Bit -- Device CLKin Select

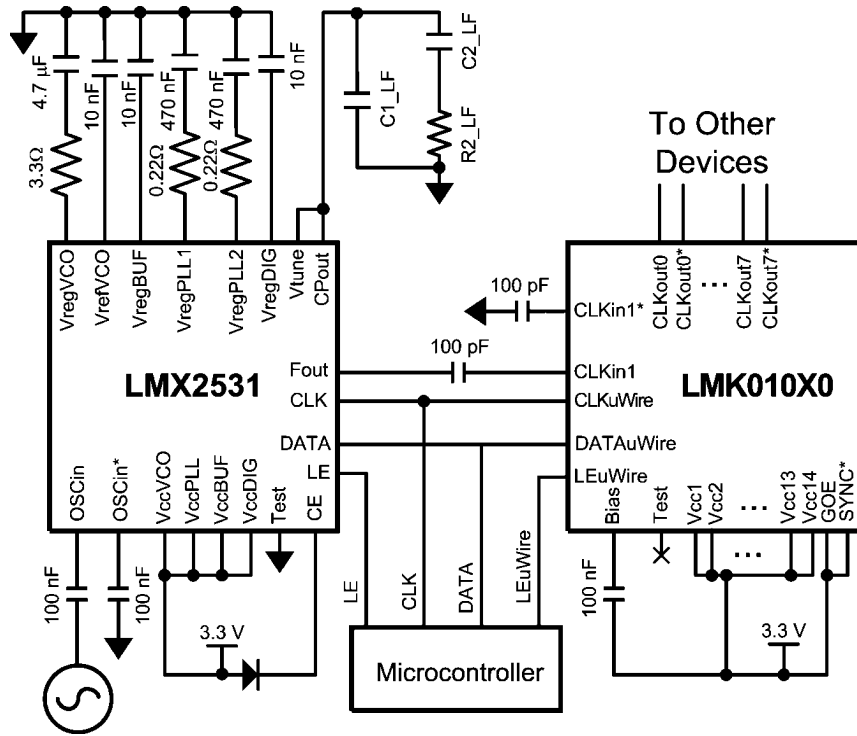
This bit determines which CLKin pin is used.

CLKin bit	Mode
0	CLKin1 (default)
1	CLKin0

3.0 Application Information

3.1 SYSTEM LEVEL DIAGRAM

The following shows the LMK01000/LMK01010/LMK01020 in a typical application. In this setup the clock may be divided, skewed, and redistributed.



30042870

FIGURE 1. Typical Application

3.2 CURRENT CONSUMPTION / POWER DISSIPATION CALCULATIONS ($V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{ C}$)

Block	Condition	Current Consumption at 3.3 V (mA)	Power Dissipated in device (mW)	Power Dissipated in LVPECL emitter resistors (mW)	
Core Current	All outputs disabled. Includes input buffer currents.	19	62.7	-	
Low clock buffer (internal)	The low clock buffer is enabled anytime one of CLKout0 through CLKout3 are enabled	9	29.7	-	
High clock buffer (internal)	The high clock buffer is enabled anytime one of the CLKout4 through CLKout7 are enabled	9	29.7	-	
Output buffers	LVDS output, Bypassed mode	17.8	58.7	-	
	LVPECL output, Bypassed mode (includes 120 Ω emitter resistors)	40	72	60	
	LVPECL output, disabled mode (includes 120 Ω emitter resistors)	17.4	38.3	19.1	
	LVPECL output, disabled mode. No emitter resistors placed; open outputs	0	0	-	
Vboost	Additional current per channel due to setting Vboost from 0 to 1.	LVPECL Output	0.5	1.65	-
		LVDS Output	1.5	5.0	-
Divide circuitry per output	Divide enabled, divide = 2	5.3	17.5	-	
	Divide enabled, divide > 2	8.5	28.0	-	
Delay circuitry per output	Delay enabled, delay < 8	5.8	19.1	-	
	Delay enabled, delay > 7	9.9	32.7	-	
Entire device CLKout0 & CLKout4 enabled in Bypassed mode	LMK01000	85.8	223.1	60	
	LMK01010	63.6	209.9	-	
	LMK01020	108	236.4	120	
Entire device all outputs enabled with no delay and divide value of 2	LMK01000	323.8	768.5	300	
	LMK01010	212.8	702.3	-	
	LMK01020	390.4	808.3	480	

From the above table, the current can be calculated in any configuration. For example, the current for the entire device with 1 LVDS (CLKout0) & 1 LVPECL (CLKout4) output in Bypassed mode can be calculated by adding up the following blocks: core current, low clock buffer, high clock buffer, one LVDS output buffer current, and one LVPECL output buffer current. There will also be one LVPECL output drawing emitter current, but some of the power from the current draw is dissipated in the external 120 Ω resistors which doesn't add to the power dissipation budget for the device. If delays or divides are switched in, then the additional current for these stages needs to be added as well.

For power dissipated by the device, the total current entering the device is multiplied by the voltage at the device minus the power dissipated in any emitter resistors connected to any of

the LVPECL outputs. If no emitter resistors are connected to the LVPECL outputs, this power will be 0 watts. For example, in the case of 1 LVDS (CLKout0) & 1 LVPECL (CLKout4) operating at 3.3 volts for LMK01000, we calculate $3.3\text{ V} \times (10 + 9 + 9 + 17.8 + 40)\text{ mA} = 3.3\text{ V} \times 85.8\text{ mA} = 283.1\text{ mW}$. Because the LVPECL output (CLKout4) has the emitter resistors hooked up and the power dissipated by these resistors is 60 mW, the total power dissipation is $283.1\text{ mW} - 60\text{ mW} = 223.1\text{ mW}$. When the LVPECL output is active, $\sim 1.9\text{ V}$ is the average voltage on each output as calculated from the LVPECL V_{OH} & V_{OL} typical specification. Therefore the power dissipated in each emitter resistor is approximately $(1.9\text{ V})^2 / 120\ \Omega = 30\text{ mW}$. When the LVPECL output is disabled, the emitter resistor voltage is $\sim 1.07\text{ V}$. Therefore the power dissipated in each emitter resistor is approximately $(1.07\text{ V})^2 / 120\ \Omega = 9.5\text{ mW}$.

3.3 THERMAL MANAGEMENT

Power consumption of the LMK01000/LMK01010/LMK01020 can be high enough to require attention to thermal management. For reliability and performance reasons the die temperature should be limited to a maximum of 125 °C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times θ_{JA} should not exceed 125 °C.

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to the printed circuit board. To maximize the removal of heat from the package a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package. A recommended land and via pattern is shown in *Figure 2*. More information on soldering LLP packages can be obtained at www.national.com.

To minimize junction temperature it is recommended that a simple heat sink be built into the PCB (if the ground plane layer is not exposed). This is done by including a copper area of about 2 square inches on the opposite side of the PCB from the device. This copper area may be plated or solder coated to prevent corrosion but should not have conformal coating (if possible), which could provide thermal insulation. The vias shown in *Figure 2* should connect these top and bottom copper layers and to the ground layer. These vias act as “heat pipes” to carry the thermal energy away from the device side of the board to where it can be more effectively dissipated.

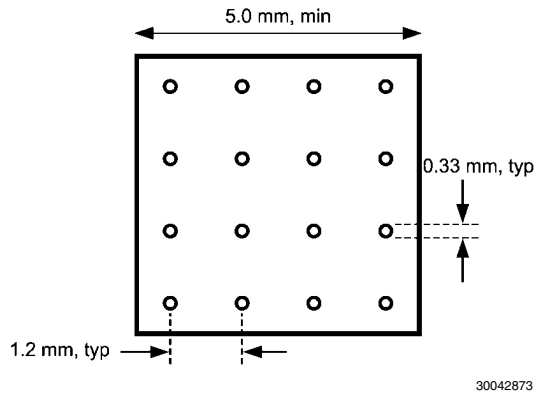
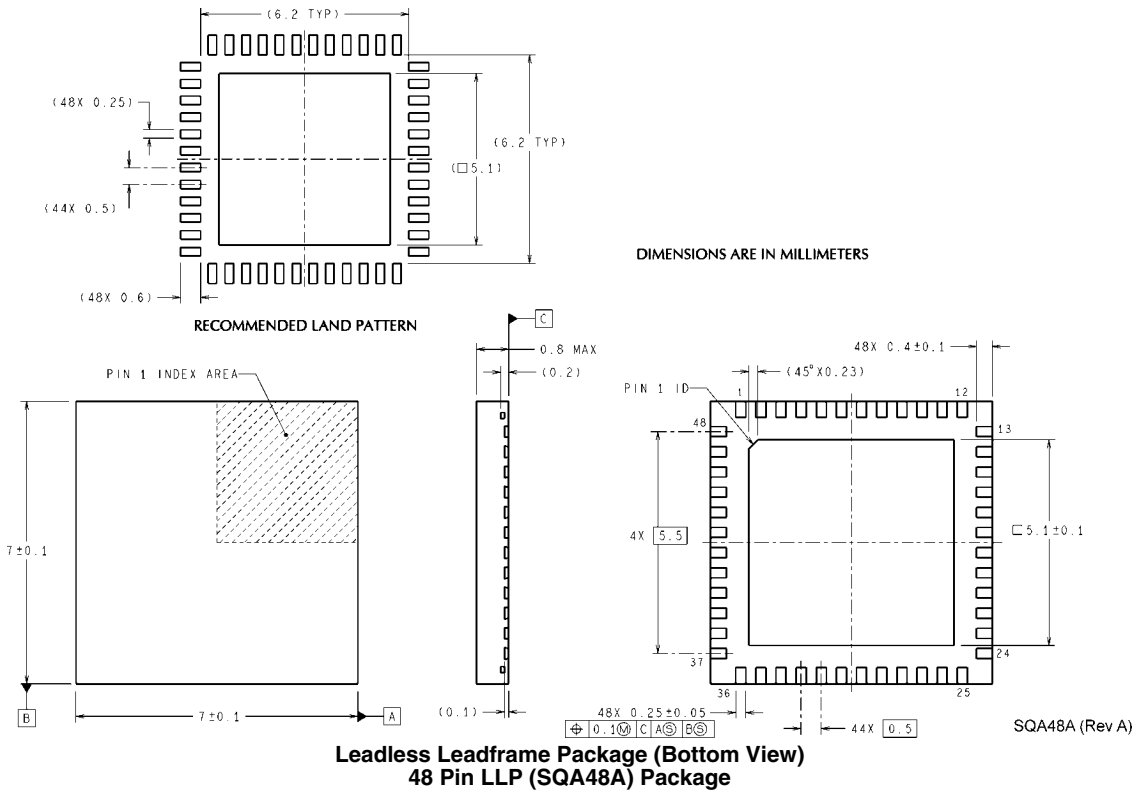


FIGURE 2. Recommended Land and Via Pattern

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number	Package Marking	Packing	LVDS Outputs	LVPECL Outputs
LMK01000ISQ	K01000 I	250 Unit Tape and Reel	3	5
LMK01000ISQX	K01000 I	2500 Unit Tape and Reel	3	5
LMK01010ISQ	K01010 I	250 Unit Tape and Reel	8	-
LMK01010ISQX	K01010 I	2500 Unit Tape and Reel	8	-
LMK01020ISQ	K01020 I	250 Unit Tape and Reel	-	8
LMK01020ISQX	K01020 I	2500 Unit Tape and Reel	-	8

Notes

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